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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **Shingo MAEDA et al.**

Art Unit: **2817**

Application Number: **10/598,419**

Examiner: **Unassigned**

Filed: **August 29, 2006**

Confirmation Number: **4383**

For: **ISOLATION TRAP CIRCUIT, ANTENNA SWITCH MODULE, AND
TRANSMISSION CIRCUIT**

Attorney Docket Number: **062481**

Customer Number: **38834**

REQUEST FOR CORRECTED FILING RECEIPT

Mail Stop: Missing Parts
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

July 2, 2008

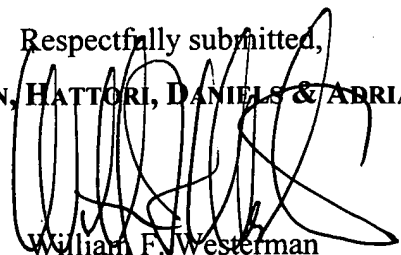
Sir:

Please supply the undersigned attorney with a corrected filing receipt for the above-identified application. The undersigned also respectfully requests that the Patent and Trademark Office records be amended to reflect the correction.

In reviewing the Official Filing Receipt, we noted an error in the **Number of Independent Claims**. The **Number of Independent Claims** should read --2--. A copy of the **Claims** is enclosed which indicates the correct information. We are also enclosing a copy of the filing receipt with the corrections highlighted.

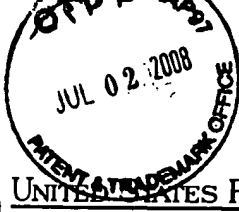
If any fees are required in connection with this paper, please charge Deposit Account No. 50-2866.

Respectfully submitted,
WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP


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WFW/pmd

Enclosures: Official Filing Receipt; Claims



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
10/598,419	08/29/2006	2817	900	062481	5	3:--2--

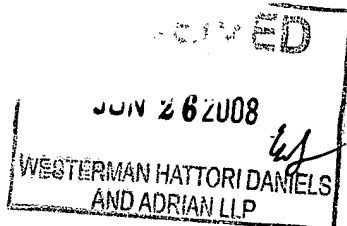
CONFIRMATION NO. 4383

FILING RECEIPT



OC000000030616026

38834
WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036



Date Mailed: 06/25/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Shingo Maeda, Osaka, JAPAN;

Assignment For Published Patent Application

SANYO ELECTRIC CO., LTD., Moriguchi-shi, JAPAN

Power of Attorney: The patent practitioners associated with Customer Number 38834

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/JP2005/000762 01/21/2005

Foreign Applications

JAPAN 2004-055787 03/01/2004

If Required, Foreign Filing License Granted: 06/21/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 10/598,419**

Projected Publication Date: 10/02/2008

Non-Publication Request: No

Early Publication Request: No

Title

Isolation Trap Circuit, Antenna Switch Module, and Transmission Circuit

Preliminary Class

333

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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What is claimed is:

[1] An isolation trap circuit in which a PIN diode PD and an inductor L are connected in parallel to a first terminal 61, and a capacitor C1 is connected in series to the inductor L, while the PIN diode PD and the capacitor C1 are connected in parallel to a second terminal 62, the isolation trap circuit being characterized in that a capacitor C2 is further connected and grounded between the first terminal 61 and the inductor L, or between the inductor L and the capacitor C1, or between the capacitor C1 and the second terminal 62.

[2] An isolation trap circuit in which a PIN diode PD and an inductor L are connected in parallel to a first terminal 61, and a capacitor C1 is connected in series to the inductor L, while the PIN diode PD and the capacitor C1 are connected in parallel to a second terminal 62, the isolation trap circuit being characterized in that a capacitor C2 is further connected and grounded between the inductor L and the capacitor C1.

[3] An antenna switch module included in a portable terminal device used in a plurality of communication systems, comprising:
a first circuit for transmitting a transmission signal of a first communication system, a second circuit for transmitting

a transmission signal of a second communication system, and a diplexer to be provided between the first circuit, the second circuit, and an antenna, the antenna switch module being characterized in that the isolation trap circuit according to claim 1 is provided in the first circuit and/or the second circuit.

[4] An antenna switch module included in a portable terminal device used in a plurality of communication systems, comprising:

10 a first circuit for transmitting a transmission signal of a first communication system and for receiving a reception signal of the first communication system, a second circuit for transmitting a transmission signal of a second communication system and for receiving a reception signal of the second communication system, and a diplexer to be provided between the first circuit, the second circuit, and an antenna, the antenna switch module being characterized in that the isolation trap circuit according to claim 1 is provided in the first circuit and/or the second circuit.

20 [5] A transmission circuit comprising a dual power amp for amplifying the first transmission signal and the second transmission signal, and the antenna switch module according to claim 3.

ABSTRACT

In an isolation trap circuit of the present invention, a PIN diode PD and an inductor L are connected in parallel to a first terminal 61, and a capacitor C1 is connected in series to the inductor L, while the PIN diode PD and the capacitor C1 are connected in parallel to a second terminal 62. The isolation trap circuit is characterized in that a capacitor C2 is further connected and grounded between the first terminal 61 and the inductor L, or between the inductor L and the capacitor C1, or between the capacitor C1 and the second terminal 62.